Jc674 U.S. PTO 09/29/99

Please type a plus sign (+) inside this box → [+]

PTO/SB/05 (4/98)
Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	PD-R98160
First Inventor or Application Identifier	Erick M. Hirata
Title	MONOLITHIC PAYLOAD IF SWITCH
Express Mail Label No.	EE578680313US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231**

Jc674 U.S. PTO 09/29/99
09/408118

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [*Total Pages* 10]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 4]
4. Oath or Declaration [*Total Pages* 3]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

**NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).*

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [X] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. [ ] Other: .....

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
    [ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: _____/_____
    Prior application information: Examiner _____ *Group / Art Unit:* _____
    For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* *or* [X] *Correspondence address below*

Name	PATENT DOCKET ADMINISTRATION				
	RAYTHEON COMPANY				
Address	P.O. Box 902				
	2000 E. El Segundo Boulevard				
City	El Segundo	*State*	CA	*Zip Code*	90245-0902
Country	USA	*Telephone*	(310) 647-2577	*Fax*	(310) 647-2616

Name (Print/Type)	Leonard A. Alkov	*Registration No. (Attorney/Agent)*	30,021
Signature	Leonard A. Alkov	*Date*	09-29-99

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

PATENT
PD R98160

MONOLITHIC PAYLOAD IF SWITCH

E. Hirata
L. F. Linder

MONOLITHIC PAYLOAD IF SWITCH

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to communication systems. More specifically, the present invention relates to switching systems used satellite communication applications.

Description of the Related Art:

Intermediate frequency (IF) crosspoint switches are used on satellites to provide routing and redundancy between data communication channels. The channels route IF signals and data in a link between antennas via the downconversion circuitry of an IF receiver and the upconversion circuitry of a radio frequency (RF) transmitter within the communications payload of the satellite.

Previously, crosspoint switches were implemented on multiple chips, typically in a 50 ohm environment and with Gallium Arsenide (GaAs) technology. The GaAs approach required GaAs switches, low noise amplifiers (LNAs) and attenuators. This also typically required the use of complementary metal-oxide semiconductor (CMOS) integrated circuits to provide selectable control of the numerous connections needed to provide redundancy and routing between the chips.

Accordingly, conventional crosspoint switches were large, heavy, expensive devices that dissipated a considerable amount of power due to the need for multiple individually packaged components that required a characteristic impedance match

interface.

In addition, as a result of using individual GaAs chips to implement an IF switch function, a large amount of routing lines were required on the board which tended to degrade channel-to-channel isolation. There were also unacceptable gain variations as a function of the output channels selected.

Hence, a need exists in the art for a low power dissipation, small, lightweight inexpensive system or method for effecting switching and routing data between channels within a satellite communications payload which provides acceptable channel-to-channel isolation and gain uniformity.

SUMMARY OF THE INVENTION

The need in the art is addressed by the crosspoint switch architecture of the present invention. The inventive architecture includes a monolithic substrate on which a plurality (N) of electrical inputs are provided. In addition, a plurality (M) of electrical outputs are provided from the substrate. A switch is disposed on the substrate for selectively interconnecting the inputs to the outputs and a control circuit is disposed on the substrate for controlling the switch. The switch comprises M, N to 1, multiplexers, each multiplexer being adapted to receive each of the N electrical inputs.

In the illustrative embodiment, each of the N inputs to each of the multiplexers is received through a respective one of N switchable amplifiers. The output of each amplifier is provided to a respective one of N switchable isolation buffers. The outputs of the buffers are summed and buffered to provide the output of each multiplexer.

The control circuit selects which input is to be passed through to the output of a given multiplexer. In the illustrative embodiment, the control circuit includes serial-in, parallel-out shift registers and decode logic circuitry.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an illustrative block diagram implementation of the crosspoint switch of the present invention.

Fig. 1a is a more detailed illustrative block diagram implementation of the controller of the crosspoint switch of the present invention.

Fig. 2 is an illustrative block diagram implementation of the active channel enable circuit of the controller of the crosspoint switch of the present invention.

Fig. 3 is an illustrative block diagram implementation of the switch matrix control circuit of the controller of the crosspoint switch of the present invention.

DESCRIPTION OF THE INVENTION

Illustrative embodiments and exemplary applications will now be described with reference to the accompanying drawings to disclose the advantageous teachings of the present invention.

While the present invention is described herein with reference to illustrative embodiments for particular applications, it should be understood that the invention is not limited thereto. Those having ordinary skill in the art and access to the teachings provided herein will recognize additional modifications, applications, and embodiments within the scope thereof and additional fields in which the present invention would be of significant utility.

Fig. 1 is an illustrative block diagram implementation of the crosspoint switch of the present invention. All of the elements of the switch 10 are disposed on a single substrate 11 and hence are implemented on a single chip. As shown in Fig. 1, the

switch 10 includes a signal distribution network 12 comprising of N dual switchable buffers 18. The N switch inputs next pass through an associated buffer amplifier 19 which fans each of the inputs, 1:M, to the M MUXes 14, one MUX per output.

In the illustrative embodiment shown in Fig. 1, N = 30 and M = 10. Those skilled in the art will appreciate that the invention is not limited to the number of channels, inputs and outputs utilized.

Each multiplexer 14 includes a plurality of multiplexers 20 and switched isolation buffers 22. Inside each MUX 14, only one of the inputs is routed to the output as determined by the control signal provided by a controller 16. The selection of one of the N inputs in the MUX is accomplished by switching one of the N switched MUX Amp's 20 on and shutting off the others using a 1 of N switch. The MUX is a voltage to current amplifier. Note that since the muxing amplifiers 20 can be shut off, the buffer amplifiers 19 (whose outputs are fanned out 1:M) will be able to drive one or all M switched MUX Amp's (when the same signal is selected in each MUX) and still maintain the gain variation within a given specification.

Each output of the isolation buffer 22 feeds into summing circuit 24. The outputs of the N switched MUX amplifiers (only one of which is active) are current summed at a low impedance function, as opposed to voltage summed, due to the large bandwidth requirement. The current from the active MUX is the only one feeding a signal to the summing junction. There are no other signal currents from the off channel inputs because they are shut off. However, these inactive MUXes are still physically connected to the summing junction and there may be feed-through from the off input channels.

To further isolate the off-channel inputs from the summing junction, the isolation buffer 22 is provided between the MUX amp output and the summing junction 24. These buffers will be turned off to shunt the undesired feed-through away from the summing junction. Finally the current is converted back into a voltage signal through another amplifier and buffered through an output amplifier 26 capable of driving into a desired input impedance (e.g. 50 ohms in the illustrative embodiment).

Fig. 1a is a more detailed illustrative block diagram implementation of the controller 16 of the crosspoint switch 10 of the present invention. In the illustrative

embodiment, the controller is implemented in complementary metal-oxide semiconductor (CMOS) technology. The controller 16 is essentially a serial-in, parallel-out (SIPO) register. For the illustrative 30 x 10 switch matrix, a series of 10, 5 bit words are shifted in and decoded to a 1 of 30 control line. The 10, 1 of 30 control lines selects which of the 30 inputs pass through to the 10 outputs.

The controller 16 includes a CMOS buffer 28, a counter 29, an active enable control circuit 30 and a switch matrix control circuit 32. The CMOS buffer 28 distributes the control signals to the counter, active channel enable and switch matrix control. The counter is enabled by the frame select and sends out a latch command every 5 clock pulses to the active channel enable and every 30 clock pulses to the switch matrix control.

Fig. 2 is an illustrative block diagram implementation of the active channel enable circuit of the controller of the crosspoint switch of the present invention. Its purpose is to provide a control that selects only the active channels per every cycle all in one circuit. The active channel enable circuit provides switch controls. The active channel enable circuit 30 sequentially samples each of the 10, 5 bit control words and decodes it to a 1 of 30 control output. These 10, 30-bit words are overlapped and stored in the same 30-bit register 34 which gives a maximum of 10 out of 30 enable signals. Those 10 signals only activate the 10 input amplifiers that are switched to the 10 outputs. Since no more than 10 inputs can be actively switched to the 10 outputs at any one time, all of the other input amplifiers are not used and are shut down to save power.

In the illustrative embodiment, the active channel enable circuit 30 includes a serial-in, parallel-out shift register 38, a set of parallel registers 39, a decoder 36 and 30-bit register 34. The decoder may be implemented with combinational logic. The decoder 36 translates a parallel input word from the registers 39 into an output signal on one of 30 control lines. The decoder output signals are latched and overlapped 10 times by the flip-flops 34 for timely output.

Fig. 3 is an illustrative block diagram implementation of the switch matrix control 32 of the controller of the crosspoint switch of the present invention. Its

purpose is to switch any one of 30 inputs to any one of 10 outputs. The matrix 32 includes a set (e.g. 50) of serial-in, parallel-out shift registers 48 that feed a set (e.g. 50) of parallel registers 46. The parallel registers 46 provide inputs to a plurality (e.g. 10) of decoders 44. The outputs of the decoder are the controls for the MUX switch matrix and are buffer by the 1 of 30 MUX drivers 42 (shown on fig.1 and 1a only).

In order to minimize crosstalk to the chip, ground lines are added between the inputs and between the output signal lines. Additionally, any signal lines on chip that need to cross over or under other signal lines will be shielded by the ground planes.

To maintain signal isolation for the IC, there should be 2 ground pads around each signal input and output.

Thus, the present invention has been described herein with reference to a particular embodiment for a particular application. Those having ordinary skill in the art and access to the present teachings will recognize additional modifications, applications and embodiments within the scope thereof.

It is therefore intended by the appended claims to cover any and all such applications, modifications and embodiments within the scope of the present invention.

Accordingly,

WHAT IS CLAIMED IS:

CLAIMS

1. A crosspoint switch architecture having:

a monolithic substrate;

a plurality (N) of electrical inputs provided on said substrate;

a plurality (M) of electrical outputs provided on said substrate;

switch means disposed on said substrate for selectively interconnecting said inputs to said outputs; and

means disposed on said substrate for controlling said switch means.

2. The invention of Claim 1 wherein said switch means further includes M multiplexers.

3. The invention of Claim 2 wherein each multiplexer is an N to 1 multiplexer and each multiplexer is adapted to receive each of said N electrical inputs.

4. The invention of Claim 3 wherein each of said N inputs to each of said multiplexers is received through a respective one of N switchable amplifiers.

5. The invention of Claim 4 wherein each multiplexer includes N selection multiplexers.

6. The invention of Claim 5 further including means for summing the outputs of said N selection multiplexers to provide a single output.

7. The invention of Claim 6 further including means for buffering said single output.

8. The invention of Claim 3 wherein each of said N inputs to each of said

multiplexers is received through a respective one of N switchable isolation buffers.

9. The invention of Claim 8 further including means for summing the outputs of said N buffers to provide a single output.

10. The invention of Claim 9 further including means for buffering said single output.

11. The invention of Claim 1 wherein said control means includes a serial in, parallel out shift register.

12. A crosspoint switch architecture having:

a monolithic substrate;

a plurality (N) of electrical inputs provided on said substrate;

a plurality (M) of electrical outputs provided on said substrate;

M multiplexers disposed on said substrate for selectively interconnecting said inputs to said outputs, each of said multiplexers being an N to 1 multiplexer, whereby each multiplexer is adapted to receive each of said electrical inputs; and

a serial in, parallel out shift register disposed on said substrate for controlling said multiplexers.

13. The invention of Claim 12 wherein each of said N inputs to each of said multiplexers is received through a respective one of N switchable amplifiers.

14. The invention of Claim 13 wherein each of said N inputs to each of said multiplexers is received through a respective one of N switchable isolation buffers.

15. The invention of Claim 14 further including means for summing the outputs of said N buffers to provide a single output.

16. The invention of Claim 15 further including means for buffering said single output.

17. A method for switching including the steps of:

providing a monolithic substrate;

providing a plurality (N) of electrical inputs provided on said substrate;

providing a plurality (M) of electrical outputs provided on said substrate;

providing M, N to 1, multiplexers on said substrate, each multiplexer being adapted to receive each of said electrical inputs, and selectively interconnecting said inputs to said outputs; and

providing a serial in, parallel out shift register on said substrate for controlling said multiplexers.

ABSTRACT OF THE DISCLOSURE

A crosspoint switch architecture (10). The inventive architecture (10) includes a monolithic substrate (11) on which a plurality (N) of electrical inputs are provided. In addition, a plurality (M) of electrical outputs are provided on the substrate (11). A switch is disposed on the substrate (11) for selectively interconnecting the inputs to the outputs and a control circuit (16) is disposed on the substrate (11) for controlling the switch. The switch comprises M, N to 1, multiplexers (14), each multiplexer (14) being adapted to receive each of the N electrical inputs. In the illustrative embodiment, each of the N inputs to each of the multiplexers is received through a respective one of N switchable amplifiers (18). The output of each amplifier (18) is provided to a respective one of N switchable isolation buffers (19). The outputs of the buffers (19) are summed and buffered to provide the output of each multiplexer (14). The control circuit (16) selects which input is to be passed through to the output of a given multiplexer (14). In the illustrative embodiment, the control circuit (16) includes a serial in, parallel out shift register and decode logic circuitry.

Fig. 1

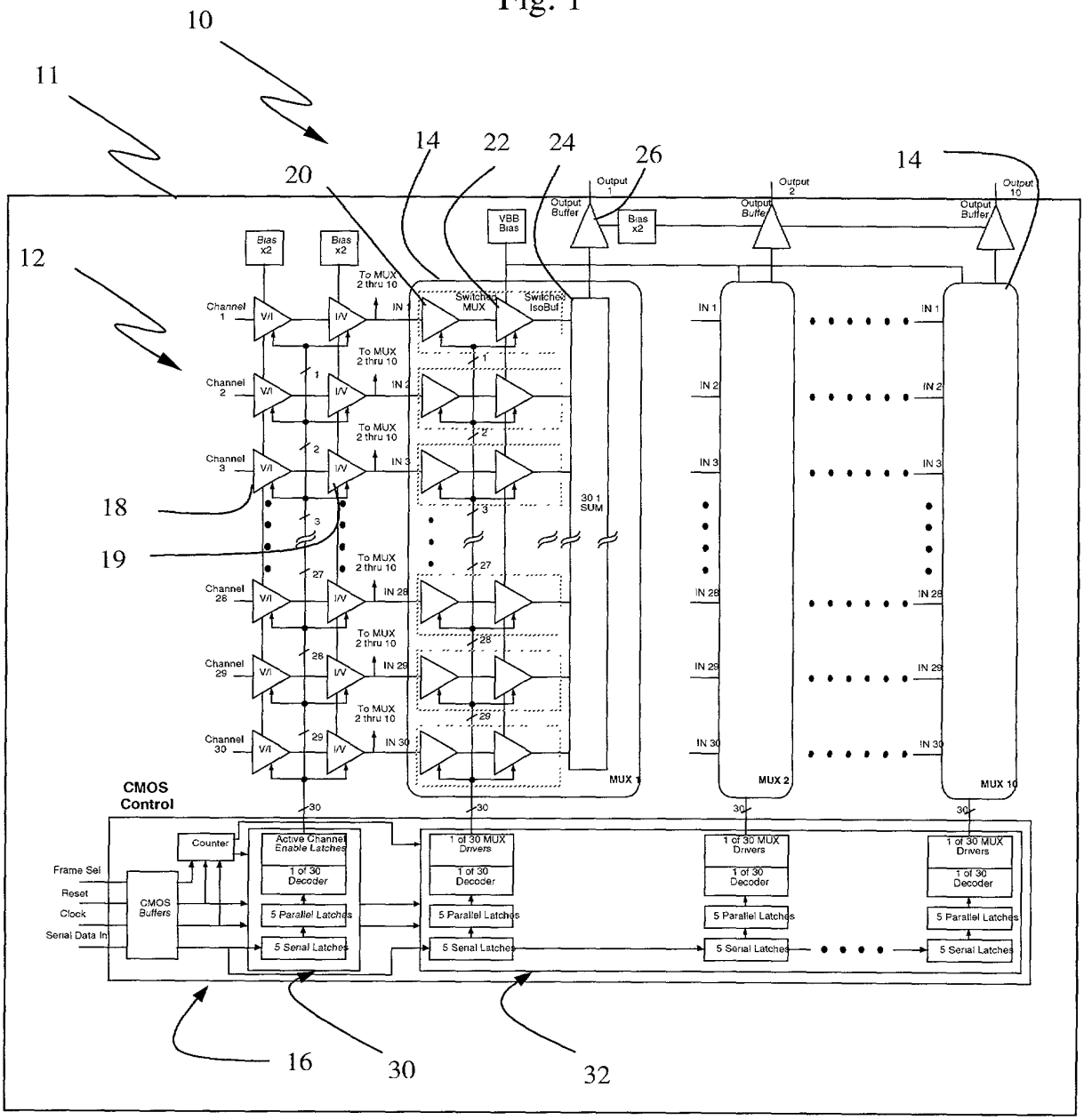

10
11
12
14
20
22
24
26
14
18
19
16
30
32
Bias x2
Bias x2
VBB Bias
Output Buffer
Bias x2
Output 1
Output 2
Output 10
To MUX 2 thru 10
Channel 1
Channel 2
Channel 3
Channel 28
Channel 29
Channel 30
V/I
I/V
IN 1
IN 2
IN 3
IN 28
IN 29
IN 30
Switched MUX
Switched IsoBuf
30 1 SUM
MUX 1
MUX 2
MUX 10
CMOS Control
Counter
Frame Sel
Reset
Clock
Serial Data In
CMOS Buffers
Active Channel Enable Latches
1 of 30 Decoder
5 Parallel Latches
5 Serial Latches
1 of 30 MUX Drivers
1 of 30 Decoder
5 Parallel Latches
5 Serial Latches

Fig. 1a

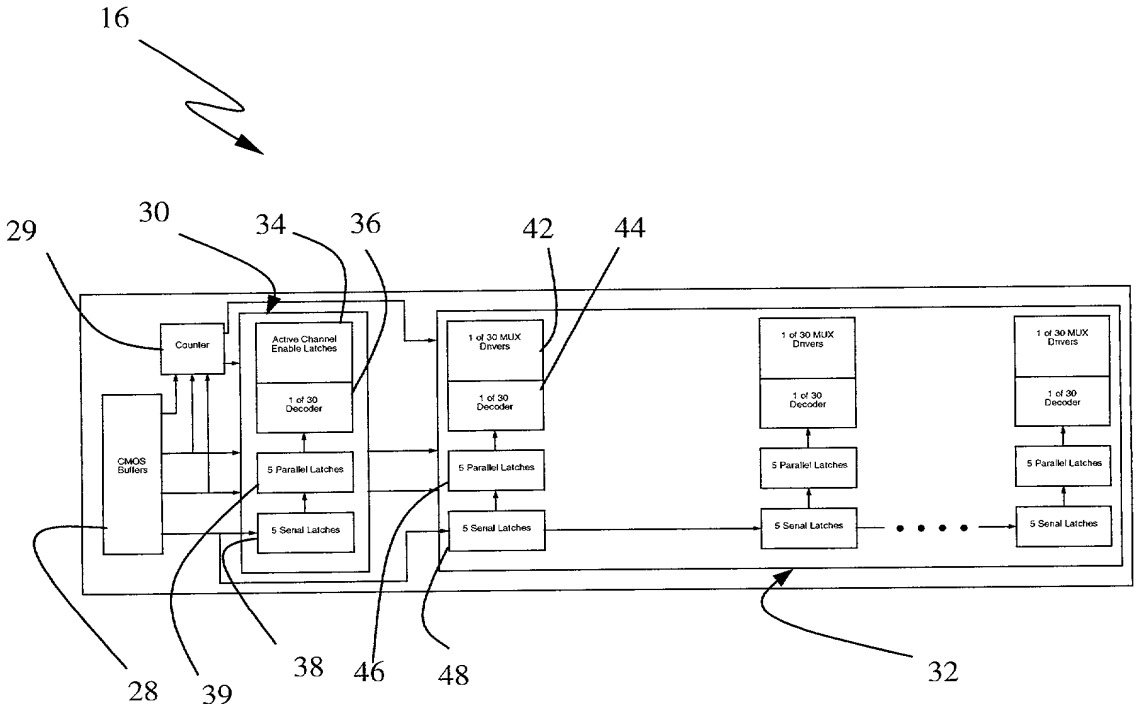

16
29
30
34
36
42
44
Counter
Active Channel Enable Latches
1 of 30 Decoder
5 Parallel Latches
5 Serial Latches
CMOS Buffers
1 of 30 MUX Drivers
1 of 30 Decoder
5 Parallel Latches
5 Serial Latches
1 of 30 MUX Drivers
1 of 30 Decoder
5 Parallel Latches
5 Serial Latches
1 of 30 MUX Drivers
1 of 30 Decoder
5 Parallel Latches
5 Serial Latches
28
39
38
46
48
32

Fig. 2

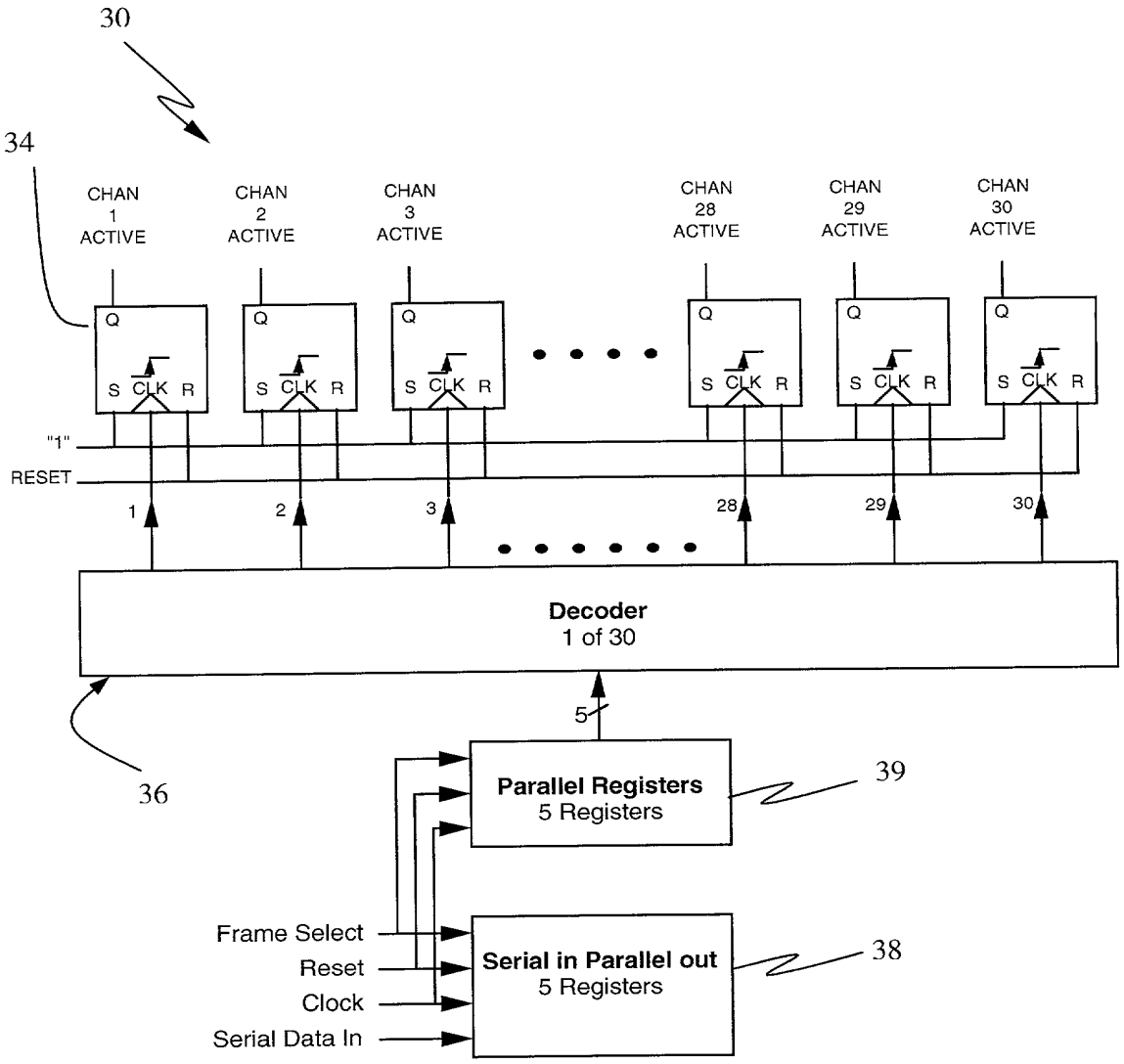
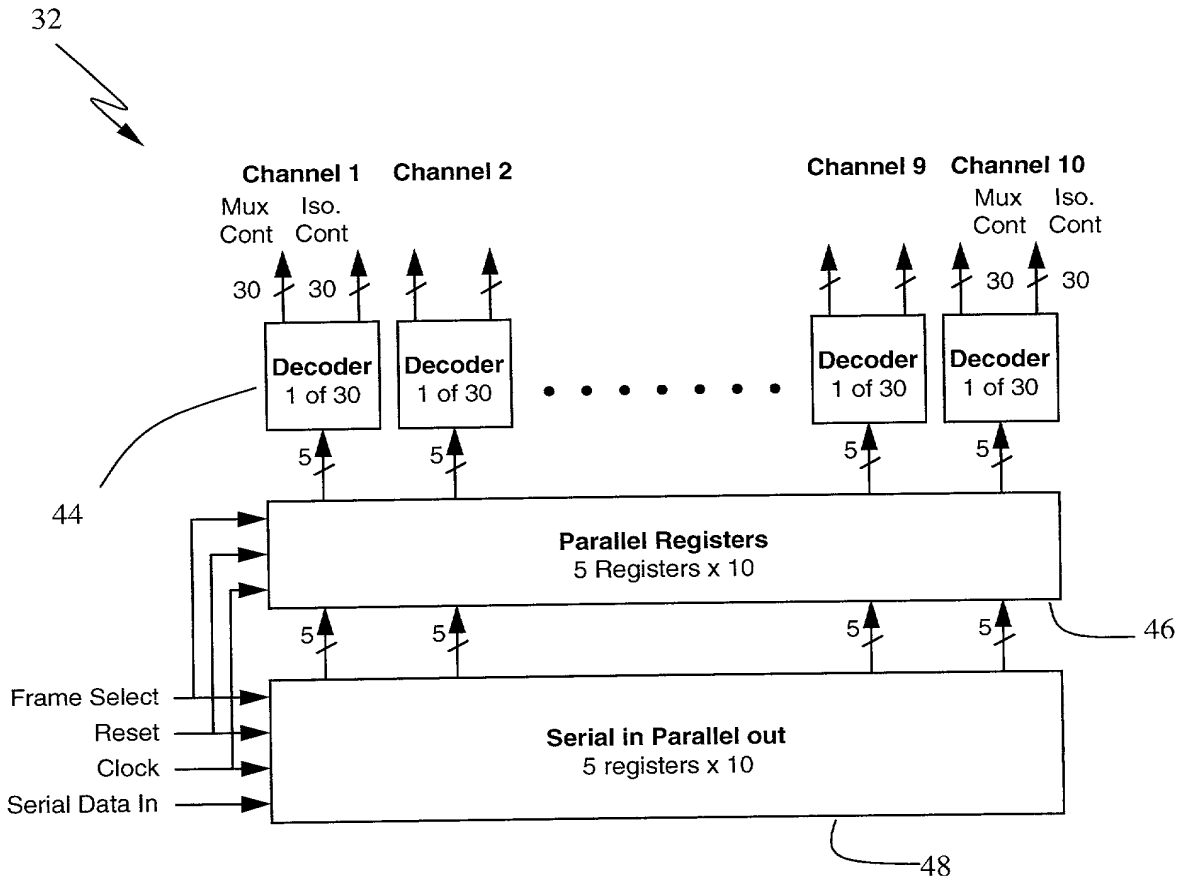

30
34
CHAN 1 ACTIVE
CHAN 2 ACTIVE
CHAN 3 ACTIVE
CHAN 28 ACTIVE
CHAN 29 ACTIVE
CHAN 30 ACTIVE
Q
S CLK R
"1"
RESET
1
2
3
28
29
30
Decoder
1 of 30
5
36
Parallel Registers
5 Registers
39
Frame Select
Reset
Clock
Serial Data In
Serial in Parallel out
5 Registers
38

Fig. 3


32
Channel 1
Channel 2
Channel 9
Channel 10
Mux Cont
Iso. Cont
30
Decoder
1 of 30
5
44
Parallel Registers
5 Registers x 10
46
Frame Select
Reset
Clock
Serial Data In
Serial in Parallel out
5 registers x 10
48

Please type a plus sign (+) inside this box → [+]

PTO/SB/01 (12-97)
Approved for use through 9/30/00. OMB 0651-0032
Patent and Trademark Office; U.S DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

[X] Declaration Submitted with Initial Filing OR [ ] Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	R98160
First Named Inventor	Erick M. Hirata
COMPLETE IF KNOWN	
Application Number	/
Filing Date	
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MONOLITHIC PAYLOAD IF SWITCH

(Title of the Invention)

the specification of which

[X] is attached hereto

OR

[ ] was filed on (MM/DD/YYYY) [ ] as United States Application Number or PCT International Application Number [ ] and was amended on (MM/DD/YYYY) [ ] (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]

[ ] Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)

[ ] Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

Burden Hour Statement: This form is estimated to take 0.4 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Please type a plus sign (+) inside this box → [+]

PTO/SB/01 (12-97)
Approved for use through 9/30/00. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

DECLARATION — Utility or Design Patent Application

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number *(if applicable)*

☐ Additional U.S or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: ☐ Customer Number [ ] → *Place Customer Number Bar Code Label here*

OR

☒ Registered practitioner(s) name/registration number listed below

Name	Registration Number	Name	Registration Number
Leonard A. Alkov	30,021		
Glenn H. Lenzen, Jr.	29,320		
Colin M. Raufer	40,781		
William C. Schubert	30,102		

☐ Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto.

Direct all correspondence to: ☐ Customer Number or Bar Code Label [ ] *OR* ☒ Correspondence address below

Name	Leonard A. Alkov, Esq.				
Address	RAYTHEON COMPANY				
Address	P.O. Box 902 (E1/E150)				
City	El Segundo	**State**	CA	**ZIP**	90245-0902
Country	U.S.A.	**Telephone**	310.647.2577	**Fax**	310.647.2616

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname
Erick M.	Hirata

Inventor's Signature						**Date**	9-29-99
Residence: City	Torrance	**State**	CA	**Country**	USA	**Citizenship**	USA
Post Office Address	21917 Ocean Avenue						
Post Office Address							
City	Torrance	**State**	CA	**ZIP**	90503	**Country**	USA

☒ Additional inventors are being named on the ____supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto

Please type a plus sign (+) inside this box → ☐

PTO/SB/02A (3-97)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

DECLARATION

ADDITIONAL INVENTOR(S)
Supplemental Sheet
Page 1 of 1

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor						
Given Name (first and middle [if any])			Family Name or Surname				
Lloyd F.			Linder				
Inventor's Signature	Lloyd F. Linder					**Date**	9-29-99
Residence: City	Agoura Hills	**State** CA	**Country** USA			**Citizenship**	USA
Post Office Address	3730 Patrick Henry						
Post Office Address							
City	Agoura Hills	**State** CA	**ZIP** 91301	**Country** USA			

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor						
Given Name (first and middle [if any])			Family Name or Surname				
Inventor's Signature						**Date**	
Residence: City		**State**		**Country**		**Citizenship**	
Post Office Address							
Post Office Address							
City		**State**		**ZIP**		**Country**	

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor						
Given Name (first and middle [if any])			Family Name or Surname				
Inventor's Signature						**Date**	
Residence: City		**State**		**Country**		**Citizenship**	
Post Office Address							
Post Office Address							
City		**State**		**ZIP**		**Country**	

Burden Hour Statement: This form is estimated to take 0 4 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231